occurrence time of a signal characteristic value of the timing signals.

REMARKS

The above identified patent application has been amended. Entry of the amendments and reconsideration and reexamination is hereby requested.

The Examiner has indicated that Claims 104 - 170 are pending. However, Claims 1 - 103 from the original issued patent have not been canceled in the Reissue Application and therefore remain pending. The Examiner in a telephone interview with the undersigned has indicted that, while not mentioned in the present Office Action, Claims 1 - 103 remain pending and allowed.

The Examiner has rejected Claims 147 - 151, 153 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Applicants have amended Claim 147 to call for (underlining added for emphasis) ... wherein the received signals are analog signals disposed in packets, each packet of the analog signals disposed in packets being divided into a first packet region comprising timing signals and a second packet region comprising data signals ...

The Applicants have also amended Claim 153 to call for (underlining added for emphasis) ... In a bidirectional communication system, a method of processing analog signal packets received through a multi-pair transmission medium, each analog signal packet including a plurality of signals having characteristic values occurring at a characteristic frequency, the method comprising ... the signals of each analog signal packet being characterized by a plurality o

f analog amplitude values, the values of the analog amplitudes defining information content, the method further comprising ... dividing <u>each analog signal packet</u> into a first <u>packet</u> region comprising timing signals and a second <u>packet</u> region comprising data signals ...

The Applicants submit that Claims 147 - 151 and 153 particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Examiner has rejected under 35 U.S.C. §103(a): Claims 104 - 118, 132, 145, 146, 152, 154 - 156, 158 - 161 as being unpatentable over Rossi in view of the admitted prior art; Claims 119, 120, 126, 127, 157, 167 and 168 as being unpatentable over Schenk in view of Townsend et al.; Claims 121 - 124, 128, 129, 162, 164 - 166 and 169 as being unpatentable over Schenk in view of Motley et al.; Claims 130, 131, 136, 137, 139, 140, 163 and 170 as being unpatentable over admitted prior art in view of Schenk.

The Applicants have canceled Claims 104 - 132, 136 - 140, 145, 146, 152, 154 - 170.

The Examiner has indicated that Claims 133, 134, 135, 141 - 144 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Applicants have amended Claims 133, 135 and 141 to be in independent form including all of the limitations of the base claim and any intervening claims. Claim 134 is dependent on Claim 133 and Claims 142 - 144 are dependent on Claim 141, and as such are allowable based upon Claims 133 and 141 respectively.

The Claim 133, 135 and 141 amendments showing brackets for deletions and underlinings for insertions are set forth below for the Examiner's convenience:

133.(twice amended) <u>A bidirectional data communication system comprising:</u>

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby;

wherein the communication signals are provided in packets, each packet comprising a preamble portion and a data containing portion, the preamble portion including timing signals; and

[A bidirectional data communication system according to claim 132,]

wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

135.(twice amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital

converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby;

[A bidirectional data communication system according to claim 131,]

the digital adaptive equalizer further comprising;

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

141. (twice amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal;

an automatic gain control circuit coupled in feedback fashion to the analog to digital converter and operatively responsive to output signals therefrom to control the gain of received communication signals; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

[A bidirectional data communication system according to claim 140,]

the digital adaptive equalizer further comprising;

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

The Examiner has also indicated that Claims 145 - 151, 153 would be allowable if rewritten to overcome the rejections under 35

U.S.C. 112, 2nd paragraph and to include all of the limitations of the base claim and any intervening claims. (Note: The Applicants believe the above-referenced Claim number "145" is a typographical error and should be "147" in view of the Examiner's rejection of Claims 145 and 146 under 35 U.S.C. §103(a)as being unpatentable over Rossi in view of the admitted prior art.)

The Applicants have amended Claims 147 and 153 as indicated above to address the rejections under 35 U.S.C. 112, 2nd paragraph and have further amended these claims to include all of the limitations of the base claim and any intervening claims. Claims 148 - 151 are dependent on Claim 147 and are believed allowable based upon Claim 147.

The Claim 147 and 153 amendments showing brackets for deletions and underlinings for insertions are set forth below for the Examiner's convenience:

147.(amended) In a bidirectional communication system, a method of processing signals received through a multi-pair transmission medium, the signals having characteristic values occurring at a characteristic frequency, the method comprising:

providing an A/D converter, coupled to receive the signals from the transmission medium;

providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals in the A/D converter at the sampling clock frequency;

generating signal samples at the sampling clock frequency, each signal sample being output from the A/D at a time assumed to correspond to the occurrence of a signal characteristic value;

processing each signal sample in a timing recovery circuit coupled, in feedback fashion, between

the output of the A/D and a sampling clock input thereto;

determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is output from the A/D at a time that actually corresponds to the occurrence of a signal characteristic value, a sampling clock phase thereby being locked to a corresponding phase of a signal characteristic value;

[The method according to claim 145, the packets of]

wherein the received signals are analog signals disposed in packets, each packet of the analog signals disposed in packets being divided into a first packet region comprising timing signals and a second packet region comprising data signals, the method further comprising:

sampling the received data signals in the A/D converter at the sampling clock frequency, wherein the data signals are sampled after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

153.(amended) In a bidirectional communication system, a method of processing analog signal packets received through a multi-pair transmission medium, each analog signal packet including a plurality of signals having characteristic values occurring at a characteristic frequency, the method comprising:

providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

predicting an occurrence time corresponding to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals at the sampling clock frequency and at the predicted occurrence time to thereby generate signal samples at the sampling clock frequency, each signal sample assumed to correspond to the occurrence of a signal characteristic value;

processing the signal samples in a high gain error generator, the high gain error generator determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is generated at a time that actually corresponds to the occurrence of a signal characteristic value, the sampling clock having an occurrence time locked in phase with a corresponding occurrence of a signal characteristic value;

[The method according to claim 152,]

the signals of each analog signal packet being characterized by a plurality of analog amplitude values, the values of the analog amplitudes defining information content, the method further comprising:

dividing each analog signal packet [the packets of analog signals] into a first packet region comprising timing signals and a second packet region comprising data signals; and

converting the analog amplitude values of the data signals to digital representations thereof by an A/D converter after the occurrence time of the sampling clock signal has been locked to the occurrence time of a signal characteristic value of the timing signals.

Support for the amendments with regard to "analog signal packets" set forth hereinabove can be found throughout the patent disclosure and, in particular, (underlining added for emphasis):

"... The signals received at the computer are provided with an automatic gain control (AGC) and then with digital conversion at a particular rate..." (Col. 2, lines 25 - 27)

"... The signals from the AGC stage 90 pass to an analog-to-digital (A-D) converter 92..." (Col. 6, lines 45 - 47)

"... The signals are in packets each having signals identifying the beginning of such packet and each having, after such identifying signals, a plurality of timing signals at the beginning of such packet ..." (Col. 5, lines 37 - 40)

Accordingly, in view of the above amendment and remarks it is submitted that the claims are now in condition for allowance and that therefore entry of the amendment and the issuance of a Notice of Allowance is hereby requested.

Respectfully submitted,

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